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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/559,757	04/27/2000	Yoshio Ozawa	04329.2306	2923

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/559,757	OZAWA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 5, 7-19* is/are pending in the application.

4a) Of the above claim(s) *8-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment C filed 9/13/2002 and entered as Paper No. 18 forms the basis of the present office action. In Amendment C Applicant substantially amended the pending claims through amendment of the independent claim 1. Applicant canceled claim 4, while claim 6 has previously been canceled in Paper No. 9, and while claims 8-19 pertain to a non-elected invention (see Election of Paper No. 7). Therefore, claims 1-3, 5 and 7 are herewith examined. Comments on Remarks by Applicant are included below in "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 9/13/2002 have been fully considered but they are not persuasive. With regard to claim 1:

(a) The post oxide film of Applicant, for all purposes related to the device application of Applicant, as opposed to the process of making application elected out per Paper No. 7, is an oxide film. So is oxide film 80 in Rhee (cf. column 7, lines 13-14). Hence, no material distinction can be allotted to oxide and post oxide in the present examination;

(b) Furthermore, with regard to the allegedly absent obviousness argument, Applicant does not specifically address the obviousness argument present on page 3, final line and page 4, first paragraph, of the previous office action (Paper No. 17), in which it was pointed out that Teramoto teaches the application of SiO_xN_y specifically for its higher dielectric strength and specifically for application as material for the gate

insulation layer. Said greater dielectric strength is a generic advantage for a gate insulation layer because said gate insulation layer is there to prevent currents from the gate to the active layer, and therefore is also an advantage in the case of Rhee, who teaches an insulated gate device (with high voltage breakdown) (cf. title and abstract, for instance). References to case law as if prima facie obviousness had not been demonstrated are therefore not persuasive.

(c) With regard to the newly added limitation through Amendment C in claim 1 it should be pointed out with reference to the abstract in Teramoto that Teramoto specifically teaches a gate insulation film of silicon, oxygen and nitrogen, with nitrogen concentration peaking in the interface between the film and the gate electrode, and hence the newly added limitation does not distinguish over precisely the teaching by Teramoto for gate insulting film composition. In view of the abstract in Teramoto the statement of Applicant on page 5, second paragraph is factually incorrect.

(d) With regard to Komori et al, in response to Applicant's statements on page 4 of Amendment C Remarks, instead of simply stating that those aspects not necessarily taught by Rhee nor Teramoto "have long been known", the examiner has given specific reasons as to why these aspects have been known and applied, as witnessed by Komori et al, with specific reference to their discussion of Figure 4 (showing rounded corners) in which Komori et al give the reason for rounding the corners of the lower edge of the gate electrode, namely that owing to such a structure the electric field can be prevented from concentrating on the corners (cf. column 6, lines 15-26), helping to

avoid dielectric (gate insulating film!) breakdown. References to case law as if prima facie obviousness had not been demonstrated are therefore not persuasive.

(e) With regard to traverses of dependent claims: they depend on the traverse of the independent claim (claim 1).

In view of the above, the examiner with regret sees no alternative but to uphold the rejections of claims 1-3, 5 and 7, in spite of arguments and Amendment C of independent claim 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-3*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee (5,646,054) in view of Teramoto (5,620,910), Komori et al (5,602,048) and Hsu et al (5,693,974).

With regard to claim 1, and with reference to Fig. 7: Rhee teaches a MOS transistor, which is a semiconductor device, comprising:

(a) a semiconductor substrate 42 (column 4, lines 1-2) having a main plane which has a first region, bordering gate insulation film 60, and a second region, bordering oxide film 80, defined in a section taken along a direction of channel length; said second region having a surface that is lower than the surface of the first region, as evidenced by Fig. 7. Furthermore, the first region

and the second region are connected to each other, because region 42 is contiguous. Also:

(b) a first gate insulating film 60 is formed on the first region (see column 4, lines 4-5);

(c) a gate electrode 62 containing silicon (in fact: made of polysilicon; see column 4, lines 5-6) is formed on 60; and

(d) an oxide film 80 (column 7, lines 13-14), arranged to be in contact with both the lower edge of the conductive film 62 and the first insulating film 60 (cf. Fig.7), is formed on the second region of the semiconductor substrate 42. Parenthetically, the difference between "oxide film" and "post oxide film" pertains to method of making hence is irrelevant for this device claim.

Rhee does not necessarily teach 60 to contain silicon, nitrogen and oxygen to take advantage of the dielectric properties of such materials, nor does Rhee teach 80 to contain silicon to take advantage of the good electrical insulation properties found among materials comprising both silicon and oxide, not does Rhee teach the nitrogen concentration in 80 to be lower than in 60. However, silicon oxynitride, a substance containing silicon, nitrogen and oxygen, has long been recognized for its excellent dielectric strength properties in connection with gate insulation layers, as evidenced by Teramoto, who teaches the application of SiO_xN_y as a thin gate insulation layer 506 (cf. Figs. 10C,F and column 18, lines 37-38) and specifically teaches the nitrogen concentration to peak within the interface between the gate and the adjacent active layer (cf. abstract; keep also in mind it is there where according to Teramoto the

nitrogen is needed in order, inter alia, to increase the dielectric breakdown strength); while Teramoto uses silicon oxide for the other insulation layers, and therefore it would have been an obvious advantage to select silicon oxynitride for this purpose. Furthermore, the use of silicon dioxide for field oxide components in the art of semiconductor devices has been well known to those of ordinary skills in the art for a long time, as witnessed by Hsu et al (cf. column 3, lines 51-55). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Rhee at the time it was made so as to include silicon, nitrogen, and oxygen in 60, and so as to include silicon and oxygen in 80.

Rhee nor Teramoto necessarily teach the lower edge of the gate electrode to be of a rounded shape. However, it has long been known and put to useful practice in the art of the invention that electric fields normal to a surface tend to be increased near curved portions, as evidenced by Komori et al, who teach (cf. Figures 3 and 4) to round off the lower edge 7E of a gate electrode in MISFET devices in semiconductor integrated circuits. The motivation by Komori et al is that "the electric field can be prevented from concentrating on the corners", which motivation can be accommodated in the invention taught by Rhee, which aims at increasing the breakdown voltage, because the maximum voltage is determined by the maximum field in the device, which can be lowered through lowering the electric field near the corners of the gate electrode where it is maximal. The inventions can be combined, because the provision of rounded corners would not interfere with any other teaching by Rhee.

With regard to the further limitation of claims 2 and 3: as detailed above, Rhee does not teach 60 to contain nitrogen, and therefore, *a forteriori,* Rhee does not teach a portion of 60 that is in contact with the semiconductor substrate to contain nitrogen at a concentration higher than the concentration in a residual portion of the first insulating film, so as to create a barrier layer within the gate insulation film. However, Teramoto teaches (see Fig. 6) a nitrogen concentration profile in the gate insulation film 306 (506) that is higher in a portion of 306 (506) that is in contact with the (active layer of the) semiconductor substrate 304 (504) than it is in a residual portion in the mid section of the gate insulating film (see column 12, lines 1-8). Parenthetically it is noted that the active layer is part of the substrate by virtue of functional necessity. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Rhee at the time it was made so as to include a nitrogen concentration profile within the gate insulation layer such that said concentration is higher in a portion that is in contact with the semiconductor substrate than in a residual portion of the gate insulation layer (gate insulating film 60 of Applicant), that is: to incorporate Applicant's claim 2. The nitrogen concentration in the portion of the gate insulation film in contact with the semiconductor substrate as taught by Teramoto preferably ranges from 1 to atomic 30 %, and thus amply exceeds the limit of 5×10^{13} cm^{-2} for the concentration per unit surface of the interface. Thus, for the same reasons as given above, it would have been obvious to one of ordinary skills in the art to carry out abovementioned modification of the invention of Rhee in such as way as to select for the concentration of nitrogen in a portion of the

gate insulating film in contact with the semiconductor substrate a value of 5 X 10^{13} cm^{-2} (*claim 3*).

3. ***Claims 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee, Teramoto, Komori et al and Hsu et al as applied to claim 1 above, and further in view of Takemura (5,917,221). As detailed above, claim 1, on which claim 5 depends, is unpatentable over Rhee in view of Teramoto, Komori et al and Hsu et al. Furthermore, the gate insulating film taught by Teramoto is a silicon oxide film containing nitrogen. Neither Rhee nor Teramoto nor Komori et al nor Hsu et al necessarily teach the gate electrode to be made of a polycrystalline silicon film containing a dopant so as to increase the gate conductivity and thereby advantageously decrease the response time, although Rhee teaches the film to be made of a polycrystalline silicon film. However, the use of dopants to achieve this improvement is well known among those skilled in the art of active semiconductor devices, as evidenced by for instance Takemura, who teaches a field effect device with a phosphorus (n-type) doped polysilicon gate (see column 10, lines 22-27). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention essentially taught by Rhee and Takemura so as to select a silicon oxide film containing nitrogen for the gate insulating film and to include a gate electrode of polycrystalline silicon containing a dopant.

4. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee, Teramoto, Komori et al, Hsu et al, and Takemura as applied to claim 5 above, and

further in view of Tomita et al (5,959,329). As detailed above, claim 5 (on which claim 7 depends) is unpatentable over Rhee, Teramoto, Komori et al, Hsu et al and Takemura, who, however, do not teach the gate insulating film as a tunnel gate insulating film to improve stress leak, dielectric breakage life, and charge trap amount characteristics, nor do they teach the conductive film as a floating electrode. However, silicon oxynitride tunnel gate insulating films are well-known in the art of oxide films for active semiconductor devices as shown by the U.S. Patent to Tomita et al, who teach a "tunnel oxide film" (see column 1, lines 6-8); however, the advantages of a silicon oxynitride film for the reasons given above (stress leak, dielectric breakage, charge trap amount characteristics) are clearly delineated (see column 2, 3-8). The examiner takes official notice that the same obviousness considerations as given above apply to a floating gate electrode as to any other gate electrode, with regard to the desirable material characteristics of the gate and its insulating surroundings, i.e., irregardless of whether the voltage is driven or floating, as enumerated above. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention essentially taught by Rhee, Teramoto and Takemura at the time it was made so as to equip the semiconductor device of claim 5 with a tunnel gate insulating film as the gate insulating film and a floating electrode as the gate electrode.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 22, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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